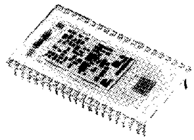
RDC-19200 MONOBRID® SERIES



10, 12, 14, OR 16 BIT INDUSTRIAL RESOLVER TO DIGITAL CONVERTERS

FULL DATA SHEET AVAILABLE

DESCRIPTION

The RDC-19200 Monobrid Series are versatile state-of-the-art resolver to digital converters featuring programmable resolution and bandwidth and a velocity output voltage.

Resolution programming allows selection of 10, 12, 14, or 16 bits and are available with commensurate accuracies up to 2 minutes +1 LSB. Resolution programming combines the high tracking rate of a 10 bit converter with the precision of a 16 bit device in one package.

The velocity output (VEL) from the RDC-19200 is a ground based voltage of 0 to ±10VDC with a linearity of 2.0% or 0.7%. VEL may be scaled up by a single external resistor to provide up to ±10VDC for the required maximum tracking rate.

APPLICATIONS

The RDC-19200 Series converters are designed for use in modern high performance commercial and industrial control systems. Applications include motor control, theodolite, radar antenna position information, CNC machine tooling, robot axis control, and process control. With their low cost and superior performance, the RDC-19200 Series converters are ideal for motion control and position monitoring applications.

FEATURES

- *LOW COST*
- *IDEAL FOR MOTOR CONTROL*
- *BUILT-IN-TEST (BIT) AND LOSS-OF-SIGNAL (LOS) OUTPUTS*
- *VELOCITY OUTPUT ELIMINATES TACHOMETER*
- *PROGRAMMABLE RESOLUTION*
- *PROGRAMMABLE BANDWIDTH*
- *ACCURACY TO ±2.3 ARC MIN.*

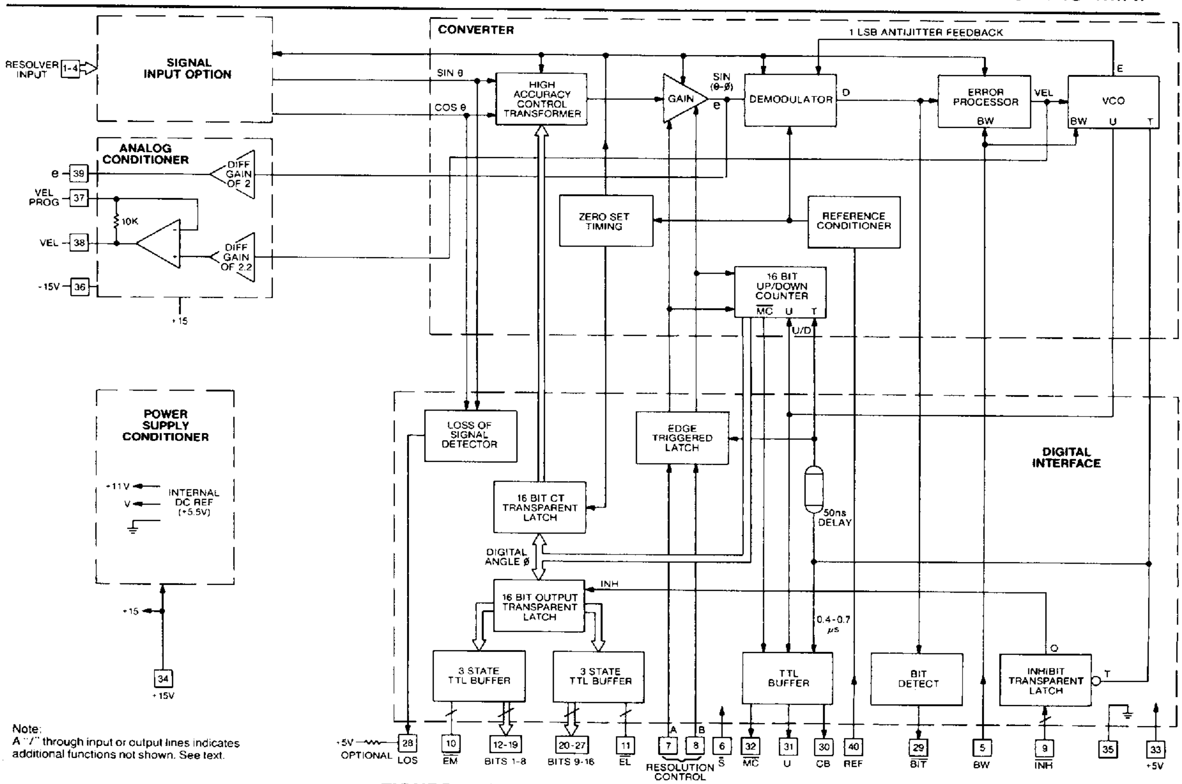


FIGURE 1. RDC-19200 BLOCK DIAGRAM

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TABLE 1. RDC-19200 SPECIFICATIONS
These specifications apply over temperature range, power supply range, reference frequency and amplitude range; ±10% signal amplitude variation and up to 10% harmonic distortion in the reference.

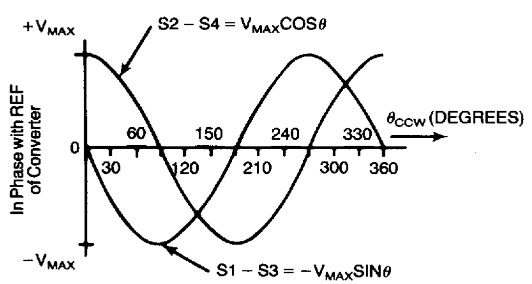
PARAMETER	VALUE	DESCRIPTION
RESOLUTION	10, 12, 14, or 16 bits	Programmable
ACCURACY GRADES	10, 8, 4, 3, 2 minutes	Max +1 LSB of selected resolution, see Ordering Information
DIFFERENTIAL LINEARITY	16, 12, 8, or 4	LSBs in the 16th bit, see Ordering Information
REPEATABILITY	1 LSB max	
REF INPUT CHARACTERISTICS		
Voltage Range	4-50Vrms	
Single Ended Input Impedance	100K Ohm min, 110K Ohm nom	
Frequency Range	360Hz to 6KHz	See Table 4, Dynamic Characteristics
SIGNAL INPUT CHARACTERISTICS		Voltage options and minimum input impedance, balanced.
Resolver	11.8V L-L	
Z_{in} Single Ended	70K Ohm	
Z_{in} Differential	140K Ohm	
Z_{in} Each line-ground	80K Ohm	
Common Mode Range	26V peak	
Max Voltage w/o damage	100V transient	
Direct	2.0V L-L	
Input Signal Type		Sin and Cos resolver signal referenced to converter's internal DC ref voltage of +5.5V.
Sin/Cos Voltage Range	2V nom, 2.3V max	
Max Voltage w/o Damage	15V continuous, 110V peak transient	
Z_{in}	>20M ohm//10pf voltage follower	
DIGITAL INPUT/OUTPUT		
Logic Type		TTL/CMOS compatible
Inputs	Logic 0 = 0.8V max Logic 1 = 2.0V min	
Max Voltage w/o Damage	−0.3 to 11V	
Loading	−10 µA max	Pull-up current source to +5V//5pf max CMOS transient protected.
$\overline{INH}$ (Inhibit)		Logic 0 inhibits, Logic 1 enables, Data stable within 0.3µs
$\overline{EM}$ (Enable bits 1-8) $\overline{EL}$ (Enable bits 9-16)		Logic 0 enables, data valid within 150 ns. Logic 1 high Z within 100 ns.
$\overline{S}$ (Control Transformer)		Logic 0 for Control Transformer, Logic 1 for normal tracking.
BW (Bandwidth)		Logic 1 = High BW (530 Hz); Logic 0 = Low BW (130 Hz)
Resolution Control		B (pin8) / A (pin 7)
10 Bit		0 / 0
12 Bit		0 / 1
14 Bit		1 / 0
16 Bit		1 / 1
		Unused output bits are at logic 0
OUTPUTS		
Parallel Data	10, 12, 14, or 16 bits	Natural binary angle, positive logic
CB (Converter Busy)		0.4 µs to 0.7 µs positive pulse; leading edge initiates counter update.
U (Direction)		Logic 1 counts up, Logic 0 counts down
$\overline{MC}$ (Major Carry)		Logic 0 at $\overline{MC}$
$\overline{BIT}$ (Built in Test)		Logic 0 for $\overline{BIT}$ condition.
LOS (Loss of Signal)		Logic 1 for LOS (1-3µA pull-up to +5V).
Drive Capability	Logic 0: 1 TTL Load Logic 1: 10 TTL Loads High Z: 10µA/5pf max	−1.6mA at 0.4V max 0.4mA at 2.8V min
ANALOG OUTPUTS		
V (Internal DC ref)	+5.5V nom	
VEL (Velocity)		See Table 6, Velocity Characteristics
e (AC error)	50mVrms per LSB of error 25mVrms per LSB of error 12.5mVrms per LSB of error 6.3mVrms per LSB of error	10 bit mode 12 bit mode 14 bit mode 16 bit mode
Dynamic Characteristics		See Table 4, Dynamic Characteristics

TABLE 1. RDC-19200 SPECIFICATIONS (Continued)				
PARAMETER	**VALUE**			**DESCRIPTION**
POWER SUPPLY CHARACTERISTICS Nominal Voltage and Range	+15VDC ±5%	+5VDC ±10%	−15VDC ±5%	Note: When analog outputs are not required, ground −15V (pin 36).
Max Voltage w/o Damage Max Current	+18V 25mA	+8V 10mA	−18V 15mA	
TEMPERATURE RANGES Operating Storage	0°C to +70°C −40°C to +120°C			
PHYSICAL CHARACTERISTICS Size Weight	1.14 x 2.02 x 0.23 inches (28.96 x 51.3 x 5.84 mm) 0.46 oz (13 gm)			40 pin TDIP

TECHNICAL INFORMATION

INTRODUCTION

The RDC-19200 Series are small, 40 pin TDIP resolver to digital hybrid converters. As shown in the block diagram (figure 1), the RDC-19200 can be broken down into the following functional parts: Signal Input Option, Converter, Analog Conditioner, Power Supply Conditioner, and Digital Interface.



Standard Resolver Control Transmitter (RX) Outputs as a Function of CCW Rotation From Electrical Zero (EZ) With R2-R4 Excited.

FIGURE 2. RESOLVER SIGNALS

SIGNAL INPUT OPTIONS

In a resolver, shaft angle data is transmitted as the ratio of carrier amplitudes across the terminals. The converter internal to the RDC-19200 operates with signals in resolver format, $\sin\theta\cos\omega t$ and $\cos\theta\cos\omega t$. Figure 2 shows the resolver signals as a function of the angle θ. The RDC-19200 accepts solid state resolver (11.8Vrms) and direct (2Vrms) inputs. The reference is a single ended input with 100K ohm impedance.

2V DIRECT INPUT OPTION. The direct inputs are transient protected voltage followers which accept 2Vrms resolver inputs, as shown in figure 3. A 2V input from a resolver allows use of a lower reference voltage. This lowers oscillator cost and allows a lower power reference oscillator.

INTERNAL DC REFERENCE VOLTAGE (V). This internal voltage is not required externally for normal operation of the converter. It is used as the internal DC reference common with the direct input option. It is nominally +5.5V and is proportional to the +15VDC supply.

11.8V RESOLVER INPUT OPTION. The 11.8V resolver inputs are true differential inputs with high AC and DC common mode rejection (see figure 4). Input impedance is maintained with power off. The recurrent AC peak + DC common mode voltage should not exceed 26V peak; maximum transient peak voltage should not exceed 100V.

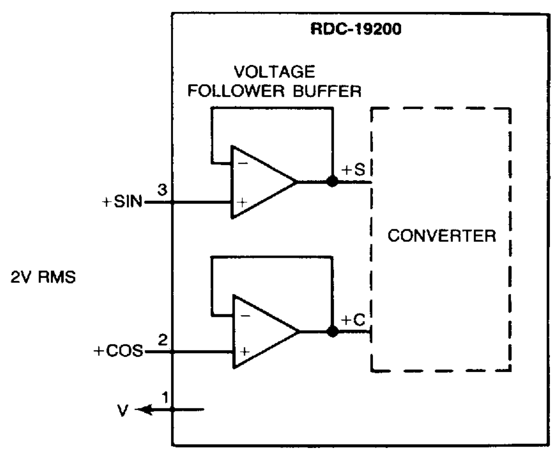


FIGURE 3. DIRECT INPUT OPTION - 2V

RESISTOR PROGRAMMING FOR NON-STANDARD INPUT VOLTAGES. When applying voltages greater than 2Vrms, a simple voltage divider can be used to attenuate both the sin and cos inputs. Since the converter inputs are voltage followers, there will be no loading on the resistor dividers (see figure 5).

The 11.8V resolver input conditioner consists of two differential amplifiers. The 11.8V input is scaled down to 2V. When applying resolver inputs greater than 11.8V, four resistors, one in series with each input line, can be used to scale down the voltage (see figure 6).

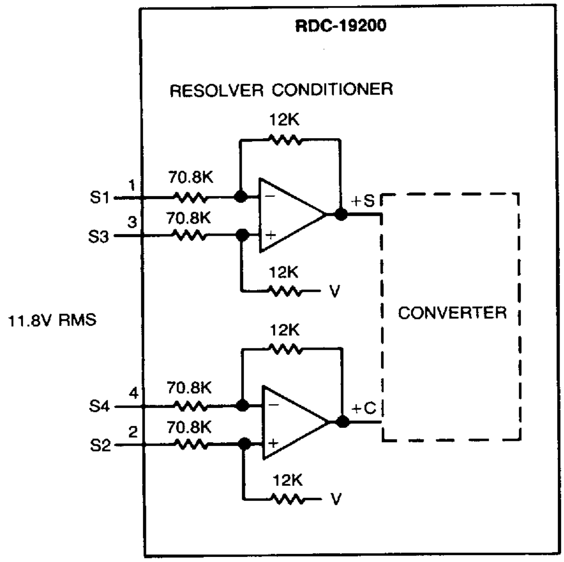
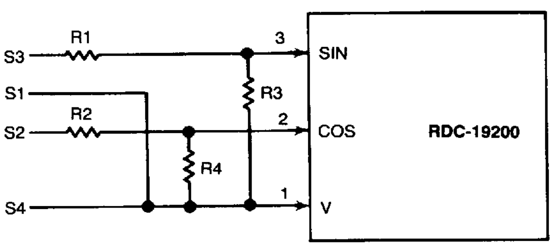


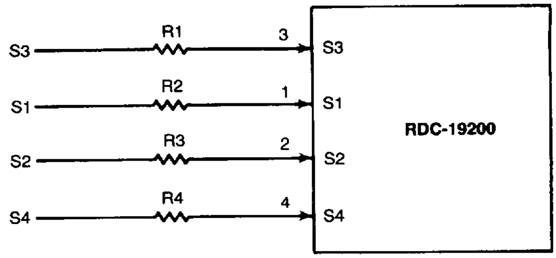
FIGURE 4. RESOLVER INPUT OPTION - 11.8V



$$\frac{\text{Input Voltage L-L}}{2V} = \frac{R1 + R3}{R3}$$

Notes:
(1) R1 = R2; R3 = R4 to 0.1% match.
(2) R1 + R3 and R2 + R4 should be as high as possible to minimize resolver loading.

FIGURE 5. INPUT RESISTOR SCALING - 2V



$$\frac{R + 70.8K}{70.8K} = \frac{\text{Input Voltage L-L}}{11.8V}$$

Notes:
(1) Input Voltage L-L is greater than 11.8V.
(2) R = R1 = R2 = R3 = R4 to 0.1% match.

FIGURE 6. INPUT RESISTOR SCALING - 11.8V

CONVERTER OPERATION

As shown in figure 1, the converter section of the RDC-19200 contains a high accuracy control transformer, demodulator, error processor, voltage controlled oscillator (VCO), up-down counter, zero-set timing, and reference conditioner. The converter produces a digital angle ϕ which tracks the analog input angle θ to within the specified accuracy of the converter.

The **control transformer** performs the following trigonometric computation:

$$\sin(\theta - \phi) = \sin\theta\cos\phi - \cos\theta\sin\phi$$

Where:

θ is angle theta, representing the resolver shaft position.
ϕ is digital angle phi, contained in the up/down counter.

The tracking process consists of continually adjusting ϕ to make $(\theta - \phi) \rightarrow 0$, so that ϕ will repeat the shaft position θ.

The output of the **demodulator** is an analog DC level proportional to $\sin(\theta - \phi)$. The **error processor** receives its input from the demodulator and integrates this $\sin(\theta - \phi)$ error signal which then drives the VCO. The VCO's clock pulses are accumulated by the **up/down counter**. The velocity voltage accuracy, linearity and offset are determined by the quality of the VCO. Functionally, the up/down counter is an incremental integrator. Therefore, there are two stages of integration which makes the converter a Type II tracking servo.

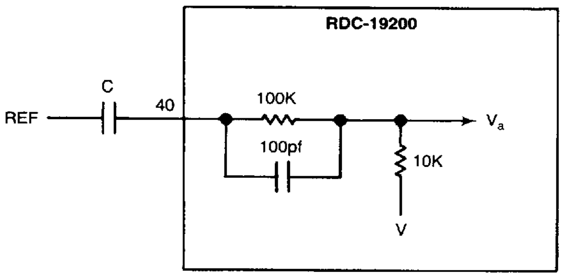
In a Type II servo, the VCO always settles to a counting rate which makes $d\phi/dt$ equal to $d\theta/dt$ without lag. The output data will always be fresh and available as long as the maximum tracking rate of the converter is not exceeded.

The RDC-19200 has unique **zero-set timing** circuits that cancel out all internal op-amp DC offsets. This zero-setting is done twice a reference input carrier cycle centered around the zero crossings. Each zero-setting cycle lasts for 18μs. During this time, the resolver input is disconnected and a zero input is switched in. The digital input to the control transformer is latched. The resultant DC error at the output of the demodulator is sampled and injected back in during the normal mode of operation.

The result is an effective way of simulating DC offset-free op-amps which ensure a converter whose actual dynamic and large signal performance is the same as its mathematical theoretical performance. In a somewhat similar manner, the velocity op-amp integrator's DC offset voltage is also cancelled out with this zero-setting scheme.

The reference conditioner is a comparator that produces the square wave reference voltage which drives the demodulator. It is single ended ground based with an input Z of 100K ohms min, 110K ohms nom, resistive.

MINIMIZING ERRORS DUE TO QUADRATURE. In those applications where highest accuracy is needed, the REF input can be phase shifted by adding a capacitor in series with the REF input (pin 40) to add a phase lead equal to the nominal phase lead of the resolver input. To determine the capacitor's value, see figure 7.



Note:
Choose C such that the V_a to REF phase lead is equal to the resolver to REF phase lead plus 9μs.

FIGURE 7. PHASE SHIFTING THE REF INPUT

QUADRATURE VOLTAGES. In a resolver, quadrature voltages are by definition the resulting 90° fundamental signal in the nulled out error voltage (e) in the converter. A digital position error will result due to the interaction of this quadrature voltage and a reference phase shift between the converter signal and reference inputs. The magnitude of this error is given by the following formula:

Magnitude of Error = (Quadrature Voltage/F.S. signal) • tan(α)

Where:

Magnitude of Error is in radians.
Quadrature Voltage is in volts.
Full Scale signal is in volts.
α = signal to REF phase shift.

An example of the magnitude of error is as follows:

Let: Quadrature Voltage = 11.8mV
Let: F.S. signal = 11.8V
Let: α = 6°
Then: Magnitude of Error = 0.35 min $\simeq$ 1 LSB in the 16th bit.

Note: Quadrature is composed of static quadrature which is specified by the resolver supplier plus the speed voltage which is determined by the following formula:

Speed Voltage = (rotational speed/carrier freq) • F.S. signal

Where:

Speed Voltage is the quadrature due to rotation.
Rotational speed is the RPS (rotations per second) of the resolver.
Carrier frequency is the REF in Hz.

ANALOG CONDITIONER

The Analog Conditioner section performs three functions. It converts analog ground from 5.5V to 0V, provides a gain of 2 for AC Error (e) and a gain of 2.2 for Velocity (VEL). The velocity scaling sensitivity can be increased with an external resistor. Refer to VEL PROGRAMMING section for more information.

POWER SUPPLY CONDITIONER

The power supply conditioner lowers the internal power supply voltage to the custom CMOS chip to +11V from the +15V supply. The +11V will track the +15V. Internal analog ground is one half of 11V or +5.5V, nom.

DIGITAL INTERFACE

The digital interface circuitry performs three main functions:

1. Latches the output bits during an Inhibit ($\overline{INH}$) command allowing stable data to be read out of the RDC-19200.
2. Furnishes parallel tri-state data formats.
3. Acts as a buffer between the internal CMOS logic and the external TTL logic.

In the RDC-19200, applying an Inhibit ($\overline{INH}$) command will lock the data in the **output transparent latch** without interfering with the continuous tracking of the converter's feedback loop. Therefore, the digital angle ϕ is always updated, and the $\overline{INH}$ can be applied for an arbitrary amount of time. The Inhibit Transparent Latch and the 50ns delay are part of the inhibit circuitry. For further information, see the INHIBIT ($\overline{INH}$, PIN 9) paragraph.

The **BIT detect** circuitry monitors the error level (D) from the demodulator and the **LOS (loss of signal) detector** detects disconnected resolver inputs.

LOGIC INPUT/OUTPUT

The digital angle outputs are buffered and provided in a two-byte format. The first byte contains the MSBs (bits 1-8) and is enabled by placing $\overline{EM}$ (pin 10) to a logic 0. Depending on the user programmed resolution, the second byte contains the LSBs and is enabled by placing $\overline{EL}$ (pin 11) to a logic 0. The second byte will contain either bits 9-10 (10 bit resolution), bits 9-12 (12 bit resolution), bits 9-14 (14 bit resolution) or bits 9-16 (16 bit resolution). All unused LSBs will be at logic 0. Table 2 lists the angular weight for the digital angle outputs.

The digital angle outputs are valid 150 ns after $\overline{EM}$ or $\overline{EL}$ are activated with a logic 0 and are high impedance within 100 ns, max after $\overline{EL}$ and $\overline{EM}$ are set to logic 1. Both enables are internally pulled up to +5V by -10μA max current sources.

TABLE 2. DIGITAL ANGLE OUTPUTS

BIT	DEG/BIT	MIN/BIT
1 (MSB ALL MODES)	180	10,800
2	90	5,400
3	45	2,700
4	22.5	1,350
5	11.25	675
6	5.625	387.5
7	2.813	168.5
8	1.405	84.38
9	0.7031	42.19
10 (LSB 10 BIT MODE)	0.3516	21.09
11	0.1758	10.55
12 (LSB 12 BIT MODE)	0.879	5.27
13	0.439	2.64
14 (LSB 14 BIT MODE)	0.0220	1.32
15	0.0110	0.66
16 (LSB 16 BIT MODE)	0.0055	0.33

Note: $\overline{\text{EM}}$ enables the 8 MSBs and $\overline{\text{EL}}$ enables the LSBs.

DIGITAL ANGLE OUTPUT TIMING

The digital angle output is 10, 12, 14, or 16 parallel data bits. All logic outputs are short-circuit proof to ground and +5V. The CB output is a positive, 0.4 to 0.7 μs pulse.

The digital output data changes approximately 50 ns after the leading edge of the CB pulse because of an internal delay (shown in figure 1). Data is valid 0.2 μs after the leading edge of CB (see figure 8). The angle is determined by the sum of the bits at logic 1.

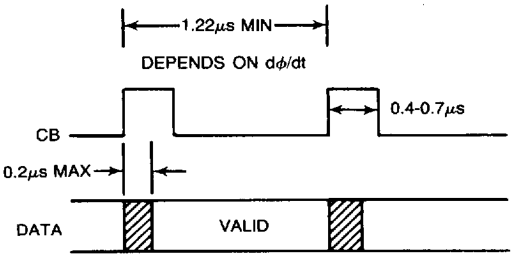


FIGURE 8. CB TIMING

INHIBIT ($\overline{\text{INH}}$, PIN 9)

When an Inhibit ($\overline{\text{INH}}$) input is applied to the RDC-19200, the Output Transparent Latch is locked, causing the output data bits to remain stable while data is being transferred (see figure 9). The output data bits are stable 0.3 μs after INH is driven to logic 0.

A logic 0 at the T input of the Inhibit Transparent Latch latches the data, and a logic 1 applied to T allows the bits to change. This latch also prevents the transmission of invalid data when there is an overlap between CB and INH. While the counter is not being updated, CB is at logic 0 and the INH latch is transparent; when CB goes to logic 1, the INH latch is locked. If CB occurs after INH has been applied, the latch will remain locked and its data will not change until CB returns to logic 0; if INH is applied during CB, the latch will not lock until the CB pulse is over. The purpose of the 50 ns delay is to prevent a race condition between CB and INH where the up-down counter begins to change as an INH is applied.

An $\overline{\text{INH}}$ input, regardless of its duration, does not affect the converter update. A simple method of interfacing to a computer asynchronous to CB is:

(1) Apply $\overline{\text{INH}}$.
(2) Wait 0.3 μs, min.
(3) Transfer the data.
(4) Release $\overline{\text{INH}}$.

As long as the converter maximum tracking rate is not exceeded, there will be no velocity lag in the converter output although momentary acceleration errors remain. If a step input occurs, as when the power is initially applied, the response will be critically damped. Figure 10 shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot (which is inherent in a Type II servo). The overshoot settling to a final value is a function of the small signal settling time.

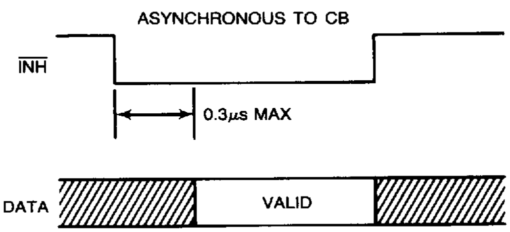


FIGURE 9. INHIBIT TIMING

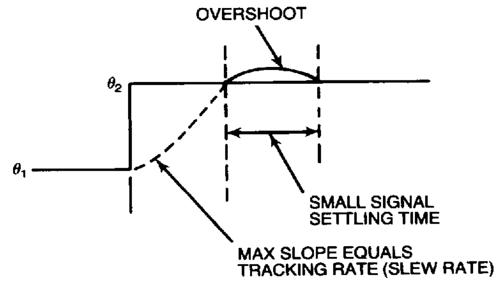


FIGURE 10. RESPONSE TO A STEP INPUT

PROGRAMMABLE RESOLUTION

Resolution is controlled by two logic inputs, A and B (see table 3). The resolution can be changed during converter operation so the appropriate resolution and velocity dynamics can be changed as needed. To insure that a race condition does not exist between counting and changing the resolution, inputs A and B are transferred through the latch internally on the trailing edge of CB (see figure 15).

TABLE 3. RESOLUTION CONTROL

B (pin 8)	A (pin 7)	RESOLUTION
0	0	10 BIT
0	1	12 BIT
1	0	14 BIT
1	1	16 BIT

Note: All unused digital output data bits are at logic 0.

FASTER SETTLING TIME USING BIT TO REDUCE RESOLUTION

Since the RDC-19200 has higher precision in the higher resolution mode and faster settling in the lower resolution modes, the $\overline{BIT}$ output can be used to program the RDC-19200 for lower resolution, allowing the converter to settle faster for step inputs. High precision, faster settling can therefore be obtained simultaneously and automatically in one unit. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

When the resolution is changed, the VEL scaling is also changed. Since the VEL output is from an integrator with a capacitor feedback, the VEL voltage cannot change instantaneously. Therefore, when changing resolution while moving, there will be a transient with a magnitude proportional to the velocity and a duration determined by the converter bandwidth (see figure 22).

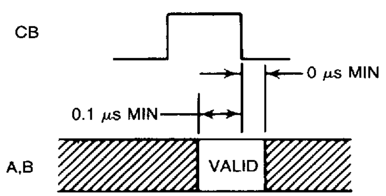


FIGURE 15. RESOLUTION CONTROL TIMING

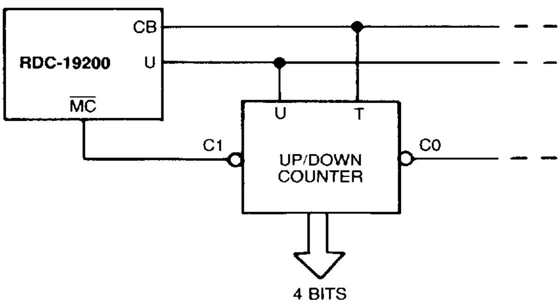
MAJOR CARRY ($\overline{MC}$, PIN 32)

Major Carry is used with Direction Output (U) for multi-turn applications. This signal is similar to the popular MSI four bit up-down counter CO (Carry Out), that is, it is normally high and goes low for all 1's when counting up or all 0's when counting down. See figure 16 for a typical interconnection.

DIRECTION OUTPUT (U, PIN 31)

Direction Output (U) is shown in figure 17. It is at logic 1 to count up and logic 0 for down. The logic level at (U) is valid at least 0.5μs before and at least 20ns after the leading edge of CB.

TURNS COUNTING



Notes:
(1) For the 4 bit up/down counter, use 74LS169B(TTL) or 4516 (CMOS).
(2) U = up/down line, logic 1 counts up.
(3) T = toggle line, counts on positive edge.

FIGURE 16. TURNS COUNTING CONNECTION DIAGRAM

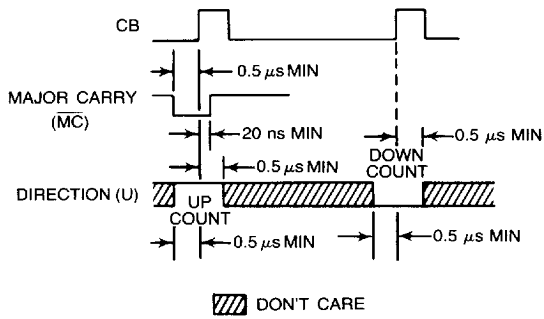


FIGURE 17. DIRECTION OUTPUT (U) TIMING

SYSTEM SELF-TEST

The RDC-19200 provides two useful logic outputs for systems self test, $\overline{BIT}$ and LOS.

BUILT-IN-TEST ($\overline{BIT}$, PIN 29)

The Built-In-Test output ($\overline{BIT}$) monitors the level of error (D) from the demodulator. D represents the difference in the input and output angles and ideally should be zero. If it exceeds approximately 65 LSBs (of the selected resolution), the logic level at $\overline{BIT}$ will change from a logic 1 to logic 0. This condition will occur during a large step and reset after the converter settles out. $\overline{BIT}$ will also change to logic 0 for an over-velocity condition because the converter loop cannot maintain input-output sync or if the converter malfunctions where it cannot maintain the loop at a null. (Note: the use of the $\overline{BIT}$ output is not recommended for 16 bit operation.)

LOSS OF SIGNAL (LOS, PIN 28)

The Loss of Signal (LOS) output is used for system safety. The LOS output changes from logic 0 to 1 if both resolver inputs are disconnected. With disconnected resolver inputs, unpredictable converter performance occurs.

If the LOS signal is used with the 2V Direct Input option, connect a 10M ohm resistor from +S to V and from +C to V. This will insure that if the input resolver signal opens, the input pin will go to V volts.

PROGRAMMABLE BANDWIDTH (BW, PIN 5)

Either low or high bandwidth can be selected by using the BW logic input. A logic 0 applied to BW selects low bandwidth (130 Hz nom), while a logic 1 selects high bandwidth (530 Hz nom). Bandwidth can be changed during converter operation.

Bandwidth and the acceleration constant (K_a) can be determined from the following formulas:

$$\text{Closed Loop Bandwidth (Hz)} = \sqrt{2}\,A/\pi$$

$$K_a = A^2$$

See Dynamic Characteristics Table 4 and figures 25 to 27 for values.

TABLE 4. DYNAMIC CHARACTERISTICS

PARAMETER	UNITS	BANDWIDTH							
		HIGH				LOW			
RESOLUTION	BITS	10	12	14	16	10	12	14	16
Input Frequency	KHz	1-6	*	2-6	NR	.36-6	*	*	2-6
Tracking Rate	RPS†	800	200	50	12.5	200	50	12.5	3.2
Bandwidth, CL	Hz	530	*	*	*	130	*	*	*
K_a	1/sec²	1.4M	*	*	*	90K	*	*	*
A_1**	1/sec	8	*	*	*	2	*	*	*
A_2**	1/sec	178	*	*	*	45K	*	*	*
A**	1/sec	1200	*	*	*	300	*	*	*
B**	1/sec	600	*	*	*	150	*	*	*
acc-1 LSB lag	°/sec²	512K	128K	32K	8K	32K	8K	2K	500
Settling time	msec	10	15	30	75	40	60	120	300

†RPS minimum
*Same as value to left
****See figure 25 for definition of A_1, A_2, A, and B.**

ANALOG OUTPUTS

The analog outputs are AC error (e) and velocity (VEL). If the analog outputs are not required, ground −15V (pin 36).

AC ERROR (e, PIN 39)

AC Error Out (e) is used in CT mode. The AC error is proportional to the difference between the resolver input angle θ and the digital input angle ϕ, $(\theta - \phi)$, with a scaling of:

50mVrms/LSB (10 bit mode)
25mVrms/LSB (12 bit mode)
12.5mVrms/LSB (14 bit mode)
6.3mVrms/LSB (16 bit mode)

The error is positive if it is in phase with the reference and negative if it is out of phase with the reference.

The e output can swing ±10V peak min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level.

VELOCITY (VEL, PIN 38)

The velocity output (VEL, pin 38) is a DC voltage proportional to angular velocity $d\theta/dt$. The velocity is the input to the voltage controlled oscillator (VCO), as shown in figure 1. Its linearity and accuracy is dependent solely on the linearity and accuracy of the VCO.

The maximum VEL output can swing ±10V min with respect to ground when the voltage level of the ±15V power supplies are 15V. The output level range changes proportionally with the power supply level. The analog output VEL characteristics are listed in table 5.

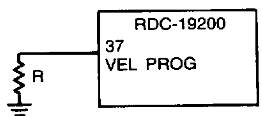
The VEL output has DC tachometer quality specs such that it can be used as the velocity feedback in servo applications.

VELOCITY PROGRAMMING (VEL PROG, PIN 37)

The velocity output scale factor can be increased by connecting an external resistor (R) from VEL PROG, pin 37 to ground. By scaling up the output, the noise and offset will increase proportionally. The value of R can be determined by the following formula:

Where: $$R = \frac{10 \times B/A}{1 - B/A}$$

R = external resistor in K Ohms
A = specified voltage scaling (RPS/VOLT)
B = desired voltage scaling (RPS/VOLT)



To determine A, refer to Table 6, Voltage Scaling.

TABLE 5. VELOCITY OUTPUT CHARACTERISTICS

PARAMETER	UNIT	RDC-19200/19202		RDC-19201/19203	
		TYP	MAX	TYP	MAX
Polarity		(positive for increasing angle)			
Voltage scaling	RPS/V	See Voltage Scaling Table 6			
Scale Factor	%	5	10	5	10
Scale Factor TC	PPM/°C	100	200	100	200
Reversal Error	%	1	2	0.5	0.7 overtemp
Linearity	% output	1	2	0.5	0.7 overtemp
Zero Offset	mV	15	40	15	40
Zero Offset TC	µV/°C	25	50	25	50
Load	KOhms	–	3	–	3
Output Voltage	V	±13	±10 min	±13	±10 min

TABLE 6. VELOCITY OUTPUT VOLTAGE SCALING (RPS/VOLT)

BW	10 BIT	12 BIT	14 BIT	16 BIT
HIGH	80	20	5	1.25
LOW	20	5	1.25	0.32

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V = \infty$) and very high acceleration constants give the RDC-19200 superior dynamic performance as listed in table 1.

* **SMALL SIGNAL STEP RESPONSE.** Figure 20 illustrates the Small Signal Step Response (100 LSB step) for low and high bandwidth for the four resolutions.

* **LARGE SIGNAL STEP RESPONSE**. Figure 21 illustrates the Large Signal Step Response (179° step) for low and high bandwidth for the four resolutions.

* **BIT OUTPUT REDUCES SETTLING TIME.** By using the $\overline{BIT}$ output together with the A and B inputs, the Large Signal Settling Time may be significantly reduced. Figure 22 shows the connections required for $\overline{BIT}$, A, and B and the resultant settling for the different resolution modes.

*VELOCITY RESPONSE

A filter on the VEL output will, for a step input in velocity, eliminate the velocity overshoot (normally critically damped) and filter carrier frequency ripple. Figure 23 shows the VEL output with and without a filter for low and high bandwidths. The VEL filter is shown in figure 24.

*TRANSFER FUNCTIONS

The dynamic performance of the converter can be determined from its transfer function block diagram (figure 25) and open and closed loop Bode plots (figures 26 and 27). Table 4 lists the parameters relating to the RDC-19200's dynamic characteristics for different resolution and bandwidth modes.

ACCURACY AND RESOLUTION

Table 7 lists the total accuracy including quantization for the various resolution and accuracy grades.

TABLE 7. ACCURACY/RESOLUTION

RDC-19200 SERIES MODEL NO.	ACCURACY	10 BIT	12 BIT	14 BIT	16 BIT
RDC-1920X-304	2' + 1 LSB	23.1	7.3	3.3	2.3
RDC-1920X-303	3' + 1 LSB	24.1	8.3	4.3	3.3
RDC-1920X-302	4' + 1 LSB	25.1	9.3	5.3	4.3
RDC-1920X-301	8' + 1 LSB	29.1	13.3	9.3	8.3

*RDC-19200 APPLICATIONS

** See Full Data Sheet*

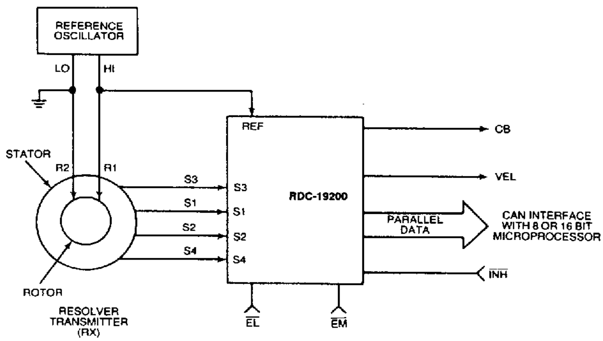


FIGURE 32. RESOLVER CONNECTION - 11.8V

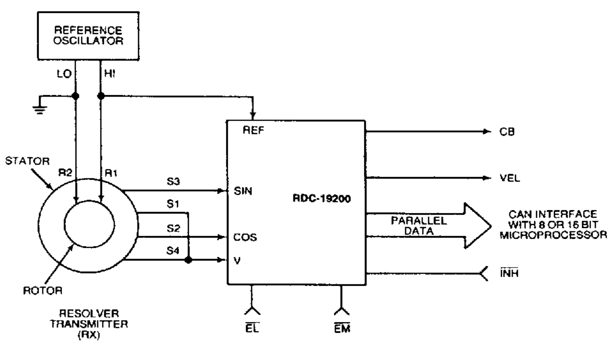


FIGURE 33. RESOLVER CONNECTION - 2V

TABLE 8. RDC-19200 PIN FUNCTIONS			
PIN NO.	TITLE	I/O	FUNCTION
1	S1(R)V(X)	I	(R) = 11.8V Resolver input; (X) = Return (DO NOT GND).
2	S2(R)+C(X)	I	(R) = 11.8V Resolver input; (X) = 2V cos input.
3	S3(R)+S(X)	I	(R) = 11.8V Resolver input; (X) = 2V sin input.
4	S4(R)−	I	(R) = 11.8V Resolver input.
5	BW	I	Bandwidth. Logic 1 for high BW (530 Hz); logic 0 for low BW (130 Hz).
6	$\overline{\text{S}}$	I	Control Transformer Set. Logic 1 for normal tracking; logic 0 for CT operation. Used when AC error (e) is needed to drive external control loop by the difference angle of the resolver input and the digital input, and for presetting the converter to a specific angle to reduce the step response time.
7 8	A B	I	Resolution Control. Changes resolution during converter operation to 10, 12, 14, or 16 bit, depending on logic level. B A Resolution 0 0 10 BIT 0 1 12 BIT 1 0 14 BIT 1 1 16 BIT
9	$\overline{\text{INH}}$	I	Inhibit. Logic 0 prevents digital output bits from changing.
10	$\overline{\text{EM}}$	I	Enable MSBs. Logic 0 enables digital output bits 1-8. Logic 1 disables these bits.
11	$\overline{\text{EL}}$	I	Enable LSBs. Logic 0 enables digital output bits 9-16. Logic 1 disables these bits.
12	1	O	Digital Output Bit 1 (MSB all modes)
13	2	O	Digital Output Bit 2
14	3	O	Digital Output Bit 3
15	4	O	Digital Output Bit 4
16	5	O	Digital Output Bit 5
17	6	O	Digital Output Bit 6
18	7	O	Digital Output Bit 7
19	8	O	Digital Output Bit 8
20	9	O	Digital Output Bit 9
21	10	O	Digital Output Bit 10 (LSB-10 BIT MODE)
22	11	O	Digital Output Bit 11
23	12	O	Digital Output Bit 12 (LSB-12 BIT MODE)
24	13	O	Digital Output Bit 13
25	14	O	Digital Output Bit 14 (LSB-14 BIT MODE)
26	15	O	Digital Output Bit 15
27	16	O	Digital Output Bit 16 (LSB-16 BIT MODE)
28	LOS	O	Loss of signal. Used for system safety, the LOS output changes from logic 0 to 1 if both resolver inputs are disconnected.
29	$\overline{\text{BIT}}$	O	Built-In-Test. Monitors level of error (D) and will change to logic 0 if it exceeds 65 bits, approx. Also logic 0 for an over-velocity condition.
30	CB	O	Converter Busy. Indicates digital output update.
31	U	O	Direction. Logic 1 to count up; logic 0 to count down.
32	$\overline{\text{MC}}$	O	Major Carry. Used for turns counting applications; normally high, goes low for all 1's when counting up or all 0's when counting down.
33	+5V	I	Supply Voltage
34	+15V	I	Supply Voltage
35	GND	–	Ground
36	−15V	I	Supply Voltage.
37	VEL PROG	I	Velocity Programming. Increases output scale factor with external resistor (R) from VEL PROG, pin 37 to ground.
38	VEL	O	Velocity. DC voltage proportional to angular velocity
39	e	O	AC Error. Used in CT mode; e is proportional to the difference between the resolver input angle θ and the digital output angle ϕ $(\theta - \phi)$.
40	REF	I	AC Reference Input. Used to drive internal demodulator.

SOURCES OF SOCKETS FOR THE RDC-19200

The following companies are sources of sockets for use with the RDC-19200 Series. Consult them for more information.

Aries Electronics, Inc. **P.O. Box 130** **Frenchtown, NJ 08825** **Tel: 1-908-996-6841**	Single In-Line Socket Strip-Line Socket Part No. 20-05511-11
Circuit Assembly Corp. 18 Thomas Street Irvine, CA 92718 Tel: 714-855-7887	Part No. CA-20-STL-XX XX-X

ORDERING INFORMATION

RDC-1920X-30 X

Accuracy

0 = 10 min +1 LSB (1)
(16 LSBs Differential Linearity, RDC-19200 and RDC-19202 only)

1 = 8 min +1 LSB
(12 LSBs Differential Linearity)

2 = 4 min +1 LSB
(8 LSBs Differential Linearity)

3 = 3 min +1 LSB
(4 LSBs Differential Linearity)

4 = 2 min +1 LSB
(4 LSBs Differential Linearity)

Configuration:

0 = 11.8V, 2% Linearity

1 = 11.8V, 0.7% Linearity

2 = 2V, 2% Linearity

3 = 2V, 0.7% Linearity

Notes:
(1) Vel and e not characterized on models RDC-19200-300 and RDC-19202-300.
(2) Differential Linearity is x LSB in the 16th bit.

I -ABR

Dimensions are inches (mm).

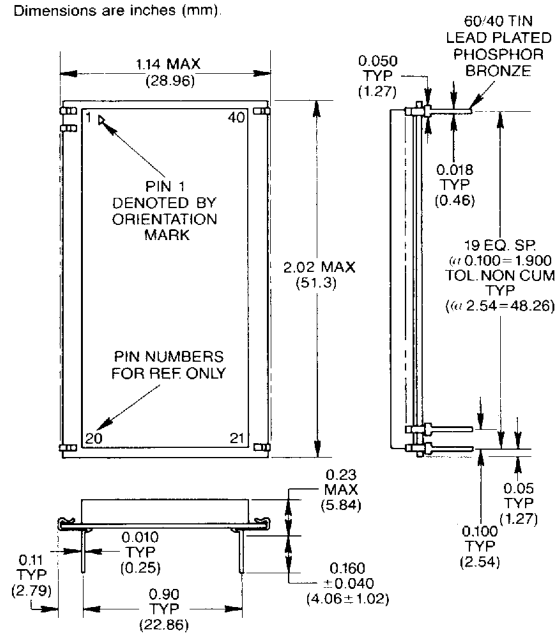


FIGURE 34. RDC-19200 MECHANICAL OUTLINE

CONNECTING THE RDC-19200

The RDC-19200 can be attached to a PC board using hand solder or wave soldering techniques. Limit exposure to 300°C (572°F) max, for 10 seconds maximum.

Do not use vapor phase soldering as this product contains SN60 or SN62 solder which melts at 180°C (356°F).

Since the RDC-19200 Series converters contain a CMOS device, standard CMOS handling procedures should be followed.